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EXAMINER	
DUONG, FRANK	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/040,166	Applicant(s) JAMES ET AL	
	Examiner Frank Duong	Art Unit 2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is a response to the preliminary amendment dated 1/5/04. Claims 1-34 are pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Perino et al (USP 6,005,895) (hereinafter "Perino").

Regarding **claim 1**, in accordance with Perino reference entirety, Perino discloses a method for inter-node communication (*FIG. 2 or 4*), comprising the steps of:

dividing a plurality of unencoded signals (*108 or in4-in0 or TABLE 3, Code (Source)*) into groups (*108 or in0, in1, in2, in3, in4 or Code(Source)*)) at a first node (*100 and 102 or 132, 133 and 134*), wherein each groups includes a portion of the unencoded signals (*Input 108 of Figure 2 or input signals in0-in4 of Figure 4*) (*see col. 4, lines 34-38 and col. 6, lines 62-64*);

transforming (*100 or 132*) each group of unencoded signals (*108 or in0, in1, in2, in3, in4 or Code(Source)*)) into a group of encoded signals (*Signal Levels or Control*

Signals) (*see col. 4, lines 31-34 and col. 6, line 64 to col. 7, line 5*), wherein each group of encoded signals (*Signal Levels or Control Signals*) has nearly an equal number of logic 1's and logic 0's (*see TABLE 2*); and

transmitting (*102 or 133 and 134*) the groups of encoded signals to a second node *(104 and 106 or 135-136 and 137)*, whereby the groups of encoded signals are transmitted with minimal current fluctuations (*see TABLE 2 and col. 3, lines 55-67 and col. 5, lines 55-59, Perino discloses the system maintains a constant current*).

Regarding **claim 2**, in addition to features recited in base claim 1 (*see rationales discussed above*), Perino further discloses wherein each group of unencoded signals includes an equal number of signals (*see TABLE 3; Code (Source)*).

Regarding **claim 6**, in addition to features recited in base claim 1 (*see rationales discussed above*), Perino further discloses selecting (*col. 4, lines 15-19 and lines 58-59*) at least one encoding scheme prior to performing the step of transforming each group of unencoded signals into a group of encoded signals (*see FIGs. 3A-3B and 5-6 for three conductors and four conductors encoding schemes*).

Regarding **claim 3**, in addition to features recited in base claim 6 (*see rationales discussed above*), Perino further discloses wherein the step of transforming each group of unencoded signals into a group of encoded signals comprises the step of transforming a group of unencoded signals (*Code(Source*)) into a group of encoded signals (Control Signals or Signal Levels) having an equal number of logic 1's and logic 0's using one of the selected at least one encoding scheme (see TABLE 3).

Regarding **claim 7**, in addition to features recited in base claim 6 (*see rationales discussed above*), Perino further discloses wherein the at least one encoding scheme transforms a group of unencoded signals to encoded signals such that a difference between a total number of unencoded data values and a total number of encoded data values is a fraction of the total number of unencoded data values (*see TABLE 4, Perino shows four signals conductors are used to transmitted three bits of data*).

Regarding **claims 4-5**, in addition to features recited in base claim 7 (*see rationales discussed above*), Perino further discloses wherein the step of transforming each group of unencoded signals into a group of encoded signals comprises the step of transforming a group of six unencoded signals into a group of eight encoded signals (*see FIGs. 2 and 4, Perino shows using three and four conductors to transmit 3 data bit. In addition, at col. 4, lines 16-19, Perino also states by adding one additional conductor, the Perino's invention triples the number of symbols that may be transmitted. Thus, it is inherent the recitation thereat reads on the claimed limitation*).

Regarding **claim 8**, in addition to features recited in base claim 1 (*see rationales discussed above*), Perino further discloses transforming (106 or 137) the groups of encoded signals received by the second node (*104 and 106 or 135-136 and 137*) back into the plurality of unencoded signals (*see col. 4, lines 50-57 and col. 7, lines 7-13* or TABLEs 3 and 6).

Regarding **claim 9**, in accordance with Perino reference entirety, Perino discloses a method for inter-node communication (*FIG. 2 or 4*), comprising the steps of:

dividing a plurality of unencoded signals (*108 or in4-in0 or TABLE 3, Code (Source)*) into groups (*108 or in0, in1, in2, in3, in4 or Code(Source)*)) at a first node (*100 and 102 or 132, 133 and 134*), wherein each groups includes a portion of the unencoded signals (*Input 108 of Figure 2 or input signals in0-in4 of Figure 4*) (*see col. 4, lines 34-38 and col. 6, lines 62-64*);

transforming (*100 or 132*) each group of unencoded signals (*108 or in0, in1, in2, in3, in4 or Code(Source)*)) into a group of encoded signals (*Signal Levels or Control Signals*) (*see col. 4, lines 31-34 and col. 6, line 64 to col. 7, line 5*), wherein each group of encoded signals (*Signal Levels or Control Signals*) has nearly a constant number of logic 1's and logic 0's (*see TABLE 2*); and

transmitting (*102 or 133 and 134*) the groups of encoded signals to a second node *(104 and 106 or 135-136 and 137)*, whereby the groups of encoded signals are transmitted with minimal current fluctuations (*see TABLE 2 and col. 3, lines 55-67 and col. 5, lines 55-59, Perino discloses the system maintains a constant current*).

Regarding **claim 10**, in addition to features recited in base claim 9 (*see rationales discussed above*), Perino further discloses wherein each group of unencoded signals includes an equal number of signals (*see TABLE 3; Code (Source)*).

Regarding **claim 12**, in addition to features recited in base claim 9 (*see rationales discussed above*), Perino further discloses selecting at least one encoding scheme prior to performing the step of transforming each group of unencoded signals into a group of encoded signals (*see FIGs. 3A-3B and 5-6 for three conductors and four conductors encoding schemes*).

Regarding **claim 11**, in addition to features recited in base claim 12 (*see rationales discussed above*), Perino further discloses wherein the step of transforming each group of unencoded signals into a group of encoded signals comprises the step of transforming a group of unencoded signals (*Code(Source)*) into a group of encoded signals (Control Signals or Signal Levels) having an equal number of logic 1's and logic 0's using one of the selected at least one encoding scheme (see TABLE 3).

Regarding **claim 13**, in addition to features recited in base claim 12 (*see rationales discussed above*), Perino further discloses wherein the at least one encoding scheme transforms a group of unencoded signals to encoded signals such that a difference between a total number of unencoded data values and a total number of encoded data values is a predetermined fraction of the total number of unencoded data values (*see TABLE 4, Perino shows four signals conductors are used to transmitted three bits of data*).

Regarding **claim 14**, in addition to features recited in base claim 9 (*see rationales discussed above*), Perino further discloses transforming (106 or 137) the groups of encoded signals received by the second node (*104 and 106 or 135-136 and 137*) back into the plurality of unencoded signals (*see col. 4, lines 50-57 and col. 7, lines 7-13* or TABLEs 3 and 6).

Regarding **claim 15**, in accordance with Perino reference entirety, Perino discloses an apparatus for inter-node communication (*FIG. 2 or 4*), comprising:

means for dividing (*not shown; inherent because of source for signal 108 or in0-in4*) a plurality of unencoded signals (*108 or in4-in0 or TABLE 3, Code(Source)*) into

groups (*108 or in0, in1, in2, in3, in4 or Code(Source)*)) at a first node (*100 and 102 or 132, 133 and 134*), wherein each groups includes a portion of the unencoded signals (*Input 108 of Figure 2 or input signals in0-in4 of Figure 4*) (*see col. 4, lines 34-38 and col. 6, lines 62-64*);

means for transforming (*100 or 132*) each group of unencoded signals (*108 or in0, in1, in2, in3, in4 or Code(Source)*)) into a group of encoded signals (*Signal Levels or Control Signals*) (*see col. 4, lines 31-34 and col. 6, line 64 to col. 7, line 5*), wherein each group of encoded signals (*Signal Levels or Control Signals*) has nearly an equal number of logic 1's and logic 0's (*see TABLE 2*); and

means for transmitting (*102 or 133 and 134*) the groups of encoded signals to a second node *(104 and 106 or 135-136 and 137)*, whereby the groups of encoded signals are transmitted with minimal current fluctuations (*see TABLE 2 and col. 3, lines 55-67 and col. 5, lines 55-59, Perino discloses the system maintains a constant current*).

Regarding **claim 16**, in addition to features recited in base claim 15 (*see rationales discussed above*), Perino further discloses means for selecting at least one encoding scheme prior to transforming each group of unencoded signals into a group of encoded signals (*see FIGs. 3A-3B and 5-6 for three conductors and four conductors encoding schemes and col. 4, lines 16-19 and 59-60*).

Regarding **claim 17**, in addition to features recited in base claim 16 (*see rationales discussed above*), Perino further discloses wherein the at least one encoding scheme transforms a group of unencoded signals to encoded signals such that a

difference between a total number of unencoded data values and a total number of encoded data values is a predetermined fraction of the total number of unencoded data values (*see TABLE 4, Perino shows four signals conductors are used to transmitted three bits of data*).

Regarding **claim 18**, in addition to features recited in base claim 16 (*see rationales discussed above*), Perino further discloses wherein the means for transforming each group of unencoded signals into a group of encoded signals comprises means for transforming (100 or 132) a group of unencoded signals (*Code(Source)*) into a group of encoded signals (Control Signals or Signal Levels) having an equal number of logic 1's and logic 0's using one of the selected at least one encoding scheme (*see TABLE 3*).

Regarding **claims 19-20**, in addition to features recited in base claim 17 (*see rationales discussed above*), Perino further discloses wherein the means for transforming each group of unencoded signals into a group of encoded signals comprises the step of transforming a group of six unencoded signals into a group of eight encoded signals (*see FIGs. 2 and 4, Perino shows using three and four conductors to transmit 3 data bit. In addition, at col. 4, lines 16-19, Perino also states by adding one additional conductor, the Perino's invention triples the number of symbols that may be transmitted. Thus, it is inherent the recitation thereat reads on the claimed limitation*).

Regarding **claim 21**, in addition to features recited in base claim 15 (*see rationales discussed above*), Perino further discloses means for transforming (106 or

137) the groups of encoded signals received by the second node (*104 and 106 or 135-136 and 137*) back into the plurality of unencoded signals (*see col. 4, lines 50-57 and col. 7, lines 7-13* or TABLEs 3 and 6).

Regarding **claim 22**, in accordance with Perino reference entirety, Perino discloses an apparatus for inter-node communication (*FIG. 2 or 4*), comprising:

means for dividing (*not shown; inherent because of source for signal 108 or in0-in4*) a plurality of unencoded signals (*108 or in4-in0 or TABLE 3, Code(Source)*) into groups (*108 or in0, in1, in2, in3, in4 or Code(Source))*) at a first node (*100 and 102 or 132, 133 and 134*), wherein each groups includes a portion of the unencoded signals (*Input 108 of Figure 2 or input signals in0-in4 of Figure 4*) (*see col. 4, lines 34-38 and col. 6, lines 62-64*);

means for transforming (*100 or 132*) each group of unencoded signals (*108 or in0, in1, in2, in3, in4 or Code(Source))*) into a group of encoded signals (*Signal Levels or Control Signals*) (*see col. 4, lines 31-34 and col. 6, line 64 to col. 7, line 5*), wherein each group of encoded signals (*Signal Levels or Control Signals*) has nearly a constant number of logic 1's and logic 0's (*see TABLE 2*); and

means for transmitting (*102 or 133 and 134*) the groups of encoded signals to a second node *(104 and 106 or 135-136 and 137)*, whereby the groups of encoded signals are transmitted with minimal current fluctuations (*see TABLE 2 and col. 3, lines 55-67 and col. 5, lines 55-59, Perino discloses the system maintains a constant current*).

Regarding **claim 23**, in addition to features recited in base claim 22 (*see rationales discussed above*), Perino further discloses means for selecting at least one encoding scheme prior to transforming each group of unencoded signals into a group of encoded signals (*see FIGs. 3A-3B and 5-6 for three conductors and four conductors encoding schemes and col. 4, lines 16-19 and 59-60*).

Regarding **claim 24**, in addition to features recited in base claim 23 (*see rationales discussed above*), Perino further discloses wherein the at least one encoding scheme transforms a group of unencoded signals to encoded signals such that a difference between a total number of unencoded data values and a total number of encoded data values is a fraction of the total number of unencoded data values (*see TABLE 4, Perino shows four signals conductors are used to transmitted three bits of data*).

Regarding **claim 25**, in addition to features recited in base claim 23 (*see rationales discussed above*), Perino further discloses wherein the means for transforming (100 or 132) each group of unencoded signals into a group of encoded signals comprises means for transforming (100 or 132) a group of unencoded signals (*Code(Source)*) into a group of encoded signals (Control Signals or Signal Levels) having an equal number of logic 1's and logic 0's using one of the selected at least one encoding scheme (see TABLE 3).

Regarding **claim 26**, in addition to features recited in base claim 22 (*see rationales discussed above*), Perino further discloses means for transforming (106 or 137) the groups of encoded signals received by the second node (*104 and 106 or 135-*

136 and 137) back into the plurality of unencoded signals (*see col. 4, lines 50-57 and col. 7, lines 7-13* or TABLEs 3 and 6).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 27-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perino.

Regarding **claims 27-34**, the claims calls for a computer program performs the steps of method claims 1, 6, 3,8, 9, 12, 11 and 14, respectively. Perino discloses the method steps of claims 1, 6, 3,8, 9, 12, 11 and 14 as discussed above, but fails to disclose the computer program. However, it is well known to translate method steps into a computer program.

It would have been obvious to those skilled in the art at the time of the invention was made, having Perino reference readily available, to translate the Perino's method steps into a computer program to arrive the claimed invention with a motivation to provide a system having the advantages provided by differential signaling, but without the inefficient ratio of the number of conductors to the number of bits transmitted (*see col. 2, first paragraph*).

Response to Arguments

4. Applicant's arguments filed 1/5/04 have been fully considered but they are not persuasive. Applicants' arguments will be addressed hereinbelow in the order in which they appear in the response filed 1/5/04.

In the Remarks of the outstanding response, on page 12 and thereinafter, pertaining the rejection of claims 1, 9, 15 and 22, Applicants argue the Perino reference does not teach "*dividing a plurality of unencoded signals into groups at a first node, wherein each group includes a portion of the unencoded signals*". To support the argument Applicants cited numerous passages in the Perino reference and concluded "*Applicant submits that sending particular permutations of signal levels across conductors to maintain a constant signal level in no way teaches "dividing a plurality of unencoded signals into groups at a first node, wherein each group includes a portion of the unencoded signals*"".

In response Examiner respectfully disagrees. Differential signaling system is well defined in IEEE Std 1596 to provide advantages, i.e. low voltage swing, self terminate, uniform ground, constant driver and link current as well as low power and EMI. However, differential signaling system requires two conductors to transmit a single bit, results in inefficient use of data interconnect resources. Recognizing the drawback of the differential signaling system, Perino sets out to invent a system having the advantages provided by differential signaling system, but using interconnect resources more efficient (col. 2, lines 1-10). In reference to Figure 4 and the description at col. 6, line 56 to col. 7, line 6 and thereinafter, Perino discloses "*translator 132 coupled to*

receive five bits of data (in4-in0). The five bits of data represent 32 different states, thereby using 32 of the 36 possible symbols. Translator 132 generates six different control signals, three of which are provided to a first driver 133 and the remaining three are provided to a second driver 134". The input signals (in4-in0) into the translator 132 are corresponding to the claimed limitation "*dividing a plurality of unencoded signals into groups at a first node, wherein each group includes a portion of the unencoded signals*". Claimed inventions/limitations are subjected to Examiner's broadest, reasonable interpretation of the prior art in the examining process. A careful review of the disputed limitation Examiner fails to recognize how the Perino's description as discussed above not read on the claimed limitation of "*dividing a plurality of unencoded signals into groups at a first node, wherein each group includes a portion of the unencoded signals*", given it the broadest reasonable interpretation.

On page 14 of the response, Applicants also argue "*Nothing in Perino teaches "transforming each group of unencoded signals into a group of encoded signals, wherein each group of encoded signals has nearly a constant, or an equal, number of logic 1's and logic 0's*".

In response Examiner respectfully disagrees. At col. 2, lines 24-27 and thereinafter Perino discloses drivers, in the differential signaling system, maintain a constant current on the multiple conductors. The constant current is maintained for all signal patterns transmitted along the conductors. There recitation thereat and thereinafter implicitly reads on the disputed limitations.

As for the argument pertaining the 103(a) rejection of claims 27-34, same rationales discussed above are Examiner's response.

Perhaps Applicants should incorporate the description of "*strobe, flag and data signals are groups and encoded*" in a manner to reduce ground-bounce during high-speed signaling (specification, page 12, second paragraph) to better reflex the Applicants' disclosed invention from that of Perino.

Examiner believes an earnest attempt has been made in addressing all of the Applicants' arguments. Due to the arguments are not persuasive and the Perino still read on the claimed invention in the present condition, the rejection from last Office Action is maintained.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

IEEE Std 1596.3, IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI), pages 1-29, 1996.

Prentice (USP 5,859,669).

Franaszek et al (USP 4,486,739).

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Frank Duong whose telephone number is (703) 308-5428. The examiner can normally be reached on 7:00AM-3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on (703) 308-5463. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Frank Duong
Examiner
Art Unit 2666

March 21, 2004